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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,426	02/05/2002	Tae Yamane	OKI.302	4137

7590 07/01/2004

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,426	YAMANE, TAE	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,9,10 and 12-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,9,10 and 12-14* is/are allowed.

6)☒ Claim(s) *5-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/09/04 has been entered. An action on the RCE follows.

2. The amendment filed on 04/30/2004 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Yamaji et al. (US Pat. 6198165).

Regarding claims 5 and 7, the APA (Fig. 1-3) discloses a resin sealed chip package/chip-size package (CSP), the CSP comprising:

- a semiconductor chip (12 in Fig. 1)
- a metal pad (14 in Fig. 1) formed on the semiconductor chip
- a wafer coat (16 in Fig. 1) formed over the semiconductor chip
- a conductive wiring pattern (18 in Fig. 1) formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;
- a molding resin (24 in Fig. 1) formed over the conductive wiring pattern
- a conductive post (20 in Fig. 1) which is formed in the molding resin and is connected to the conductive wiring pattern
- a terminal (22 in Fig. 1) which is formed on the molding resin and is connected to the conductive post
- a connecting portion directly between the conductive wiring pattern and the conductive post (see Fig. 3)

(Fig. 1-3; specification pages 7-9).

The APA fails to teach:

a) the connecting portion having a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern, and

b) a dummy pattern arranged adjacent the first and second boundaries and along sides of the connecting portion.

a) The APA in Fig. 4 further teaches the CSP having the connecting portion (CP) where the CP has a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern (APA: specification pages 8 and 9).

b) Yamaji et al. teach a CSP having a number of dummy wiring patterns having a variety of configurations where the dummy wiring patterns having two regions/parts being arranged (see a layout of patterns 14 having large and small patterned areas on left side of the connecting portion and CP and large patterned area on right side of the same in Fig. 2; Col. 6, line 14- Col. 7, line 35) adjacent along two/both sides of a connecting portion (not numerically referenced- see connecting portion between 8 and 10 in Fig, 2) between a conductive wiring pattern and an external connecting electrode/conductive post (8 and 10 respectively in Fig. 2) to improve the planarization and adhesion of an insulating layer and to minimize associated defects (Col. 7, lines 1- 35). Yamaji et al. further teach the two regions/parts being arranged (see the layout of 14 with respect to 8 in Fig. 2) along the conductive wiring pattern.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the elements a0 and b) as taught by the APA and Yamaji et al. so that the adhesion of the insulating layer can be improved and the defect level can be reduced in the APA's CSP.

Regarding claim 6, forming the dummy pattern during a same process as the conductive wiring pattern and arranging parallel to the same do not distinguish over the APA and Yamaji et al., because only the final product/structure is relevant, not the process or the sequence of forming and arranging the dummy pattern such as "before/after depositing the conductive pattern" or "during sputtering or any other process step". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Response to Arguments

5. Applicant's arguments with respect to claims 5-7 have been considered but are moot in view of the new ground(s) of rejection.

Allowabl Subject Matter

6. Claims 1-3, 9, 10 and 12-14 are allowed.

Reasons for Allowance

7. The following is an examiner's statement of reasons for allowance:

The references of record do not teach either singularly or in combination at least the limitations "the connecting portion having a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern, wherein a dent is formed at and around the connecting portion" as recited in the independent claim 9, and "the connecting portion having a width that gradually decreases from a first boundary at the conductive post to a second boundary at the conductive wiring pattern, the connecting portion having a first region extending outwardly from the conductive post and a second region extending in a perpendicular direction from the first region, the second region extending from the connecting portion" as recited in the independent claim 12 in a chip size semiconductor package having a connecting portion between the wiring pattern and a conductive post where the conductive post being formed in a molding resin.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

06-26-04

NITIN PAREKH

PATENT EXAMINER

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